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Document ID: US 20020014691 A1 Issue Date: 20020207 Pages: 16 Title: MULTIPLE LINE GRID ARRAY PACKAGE Current OR: 257/697

Document ID: US 6315200 B1 Issue Date: 20011113 Pages: 296 Title: Encoded data card reading system Current OR: 235/454

Document ID: US 6204562 B1 Issue Date: 20010320 Pages: 6 Title: Wafer-level chip scale package Current OR: 257/777

Document ID: US 6093243 A Issue Date: 20000725 Pages: 154 Title: Semiconductor device and its fabricating method Current OR: 117/8

Document ID: US 6066872 A Issue Date: 20000523 Pages: 153 Title: Semiconductor device and its fabricating method Current OR: 257/309

Document ID: US 6043109 A Issue Date: 20000328 Pages: 7 Title: Method of fabricating wafer-level package Current OR: 438/113

Document ID: US 5994766 A Issue Date: 19991130 Pages: 12 Title: Flip chip circuit arrangement with redistribution layer that minimizes Current OR: 257/659

Document ID: US 5879447 A Issue Date: 19990309 Pages: 152 Title: Semiconductor device and its fabricating method Current OR: 117/8

Document ID: US 5582640 A Issue Date: 19961210 Pages: 154 Title: Semiconductor device and its fabricating method Current OR: 117/8

Document ID: US 5391912 A Issue Date: 19950221 Pages: 36 Title: Semiconductor device having polycrystalline silicon region forming a Current OR: 257/588

Document ID: US 5227660 A Issue Date: 19930713 Pages: 37 Title: Semiconductor device Current OR: 257/588

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L1: [2237] semiconductor and redistribution
L2: [292] 1 and peripheral
L3: [0] 2 and "interconnect line"
L4: [13] 2 and "line width"
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I041 "quad flat pack"

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2 and "line width"
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U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	US 20020014691 A1	20020207	16	MULTIPLE LINE GRID ARRAY PACKAGE	257/697	
2	<input type="checkbox"/>	US 6315200 B1	20011113	296	Encoded data card reading system	235/454	235/462.01; 235/462.1; 235/462.2;
3	<input type="checkbox"/>	US 6204562 B1	20010320	6	Wafer-level chip scale package	257/777	257/723; 257/775;
4	<input type="checkbox"/>	US 6093243 A	20000725	154	Semiconductor device and its fabricating method	117/8	117/9; 438/250;
5	<input type="checkbox"/>	US 6066872 A	20000523	153	Semiconductor device and its fabricating method	257/309	257/534
6	<input type="checkbox"/>	US 6043109 A	20000328	7	Method of fabricating wafer-level package	438/113	438/109; 438/118
7	<input type="checkbox"/>	US 5994766 A	19991130	12	Flip chip circuit arrangement with redistribution layer that minimizes	257/659	257/664; 257/691
8	<input type="checkbox"/>	US 5879447 A	19990309	152	Semiconductor device and its fabricating method	117/8	117/9; 117/930
9	<input type="checkbox"/>	US 5582640 A	19961210	154	Semiconductor device and its fabricating method	117/8	117/930; 438/166;
10	<input type="checkbox"/>	US 5391912 A	19950221	36	Semiconductor device having polycrystalline silicon region forming a	257/588	257/486; 257/627;
11	<input type="checkbox"/>	US 5227660 A	19930713	37	Semiconductor device	257/588	257/577; 257/627;

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